synaptics

DHAN-TE Module DECT ULE Platform Datasheet

PN: 505-001248-01 Rev A

Contents

List of Figures

List of Tables

1. Introduction

1.1. General Description

DSP Group's DHAN-TE module is based on the state-of-the-art DHX101, a 4th generation DECT System on a Chip (SoC). The DHAN-TE module is well suited for all DECT and ULE device applications. The DHAN-TE software stack includes standard DECT ULE MAC-PHY connectivity as well as HAN-FUN (ULE Alliance standard) functionality for Dual-Mode (data and audio) ULE. The application software written by the customer typically runs atop the communication stack running on the DHX101 within the DHAN-TE. However, the application Host can also run on an external MCU that communicates with the DHAN-TE via a UART interface.

1.2. Features

- Excellent radio performance, with over 119dB system gain
- Radio covers all regional DECT bands with a simple re-configuration of the EEPROM
- Fully compliant with regulatory standards
- Compact dimensions: 27.2x16.9x3.3mm (including the RF shield height)
- Minimized external BOM
- Operating temperature: -40°C to 85°C

1.3. Block Diagram

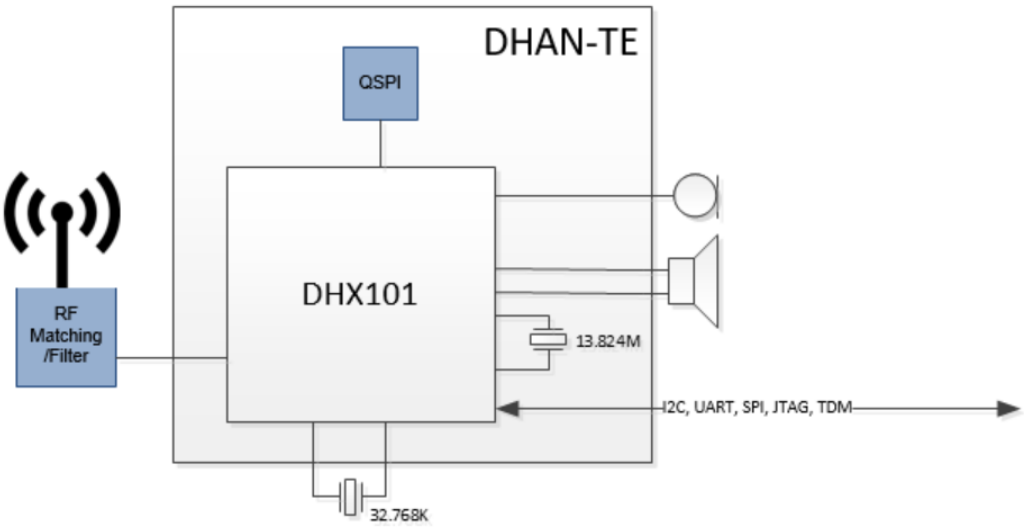

Figure 1. DHX101 DHAN-TE Module Block Diagram

2. Pin and Signal Description

Figure 1 and Table 1 show the detailed pin diagram and descriptions.

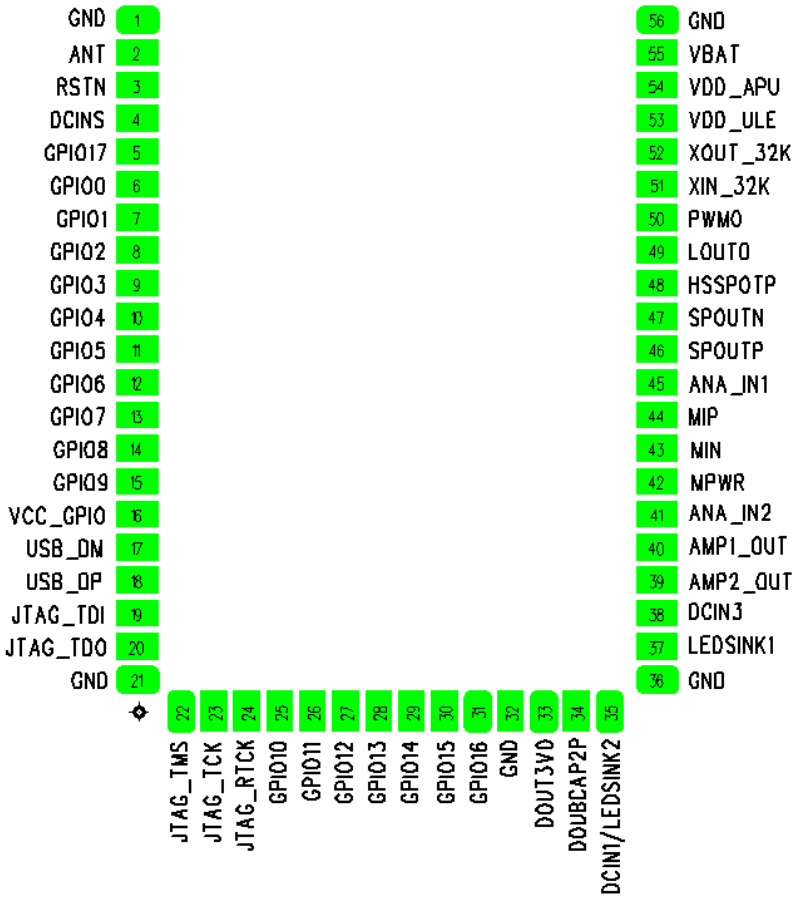

Figure 2. DHAN-TE Module Pin Diagram

Table 1. DHAN-TE Module Pin Description

Pin No.	Name	Description/Type
1	GND	GND
2	ANT	Antenna Port. Route to external antenna
3	RSTN	For standalone operation, shunt this pin to GND with 100nF. For an application running on an external MCU, this pin should be connected to a Host MCU IO and used to reset the DHAN-TE
4	DCINS	Leave NC
5	GPIO17	—
6	SCL (GPIO0)	GPIO or I2C Clock. Open Drain, reset value is floating. Leave NC if not used.
7	SDA (GPIO1)	GPIO or I2C Data. Open Drain, reset value is floating. Leave NC if not used.
8	GPIO2	GPIO or TDM_TXD
10	GPIO4	GPIO or TDM_FSYNC

Pin No.	Name	Description/Type
11	GPIO5	GPIO or TDM_FSYNC
12	GPIO6	GPIO or SPI Data In. Leave NC if not used
13	GPIO7	GPIO or SPI Data Out. Leave NC if not used
14	GPIO8	GPIO or SPI Clock
15	GPIO9	GPIO or UART Rx or SPI Chip Select
16	VCC_GPIO	Input. Sets the IO Logic level at the module interface at 1.8 or 3V.
17	USB_DM	—
18	USB_DP	—
19	TDI	JTAG Data In. Connect to TP
20	TDO	JTAG Data Out. Connect to TP
21	GND	—
22	TMS	JTAG Mode Select. Connect to TP
23	TCK	JTAG Clock. Connect to TP
24	RTCK	JTAG Reset. Connect to TP
25	GPIO10	GPIO or UART Tx
26	GPIO11	GPIO
27	GPIO12	GPIO
28	GPIO13	GPIO
29	GPIO14	GPIO
30	GPIO15	GPIO
31	GPIO16	GPIO
32	GND	—
33	DOUT3V0	3V (Doubler) Output. While DHAN-TE is hibernating, this pin is either in tristate (default SW configuration) or pulled to GND. Can be used in conjunction with GPIO7 and 8 above to drive a LED or button during non-hibernation modes
34	DOUBCAP2P	Pull down with 1M resistor
35	LEDSINK2/DCIN1	ULE I/O. Leave NC if not used
36	GND	GND
37	LEDSINK1/PWM	—
38	DCIN3	ADC input used to monitor power supply input
39	AMP2_OUT	ULE I/O. Typically used (as input) to wake up the DHAN-TE from hibernation
40	AMP1_OUT	ULE I/O. Typically used (as output) to indicate DHAN-TE is active (logic high)
41	ANA2_IN	ULE I/O. During hibernate, Logic High should not be applied to this pin (it can result in leakage current). Leave NC if not used
42	MPWR	Microphone Power
43	MIN	Leave NC if not used
44	MIP	Leave NC if not used
45	ANA_IN1	ULE I/O. Leave NC if not used
46	SPOUTP	Speaker Output, Positive
47	SPOUTN	Speaker Output, Negative
48	HSSPOTP	Headset Speaker Out, Positive

Pin No.	Name	Description/Type
49	LOUT	Headset Speaker Out, Negative
50	PWM0	Analog Output
51	XIN_32K	Connect to 32.768 XTAL
52	XOUT_32K	Connect to 32.768 XTAL
53	VDD_ULE	1.8V output. Active during hibernate. Can be used to power VCC_GPIO (Pin16)
54	VDD_APU	1.8V Test Point. Leave NC
55	VBAT	Power Supply Input. Connect to battery or regulated 3V supply
56	GND	GND

3. Electrical Specifications

Unless otherwise noted, all specifications are for 25°C.

3.1. Absolute Maximum Ratings

- Minimum voltage applied to all pins: -0.3V
- Maximum voltage applied to all pins: +4.6V
- Storage temperature range: -45 to +90°C

Note: Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

3.2. Recommended Operating Conditions

Table 2. Recommended Operating Conditions

Rating	Conditions	Min	Typ	Max	Unit
Operating ambient temperature	—	-40	+25	+85	°C
VBAT	—	1.95	3.0	3.6	V
All GPIOs Condition: VCC_GPIO is 3V	VIL VIH VOL VOH	2.0 2.4	—	0.8 0.4	V
All GPIOs Condition: VCC_GPIO is 1.8V	VIL VIH VOL VOH	1.17 1.35	—	0.63 0.45	V
RSTN	VIL VIH	0.6*VBAT	—	0.3*VBAT	V
DCIN3	—	1.95	3.0	VBAT	V

VBAT=3V

Table 3. Peak and Hibernation Currents

Parameter	Test Conditions	Typ	Max	Unit
Tx Current	Band=EU @ 23dBm	400	480	mA
Tx Current	Band=US @ 21dBm	250	300	mA
Rx Current	Max Gain Setting	125	135	mA
Paging Current	1s response latency	90	—	µA
Hibernation Current	—	2	—	µA

3.3. Transmitter

VBAT=3V

Table 4. Tx Characteristics

Characteristics	Test Conditions	Min	Typ	Max	Unit
NTP	Band=EU	21.5	23	24	dBm
NTP	Band=US	19	20	21	dBm
Harmonics	Band=EU & US	—	-40	-35	dBm
Transmission Mask	EN 301406 Paragraph 5.3.3	—	Comply	—	N/A
Frequency Offset	EN 301406 Paragraph 5.3.1	-50	8	+50	KHz
Frequency Drift	EN 301406 Paragraph 5.3.5	-15	0	+15	KHz/Slot
Emission Due Modulation	EN 301406 Paragraph 5.3.6.2 M±1 M±2 M±3 M>±3	—	 -20 -42 -47 -50	 -8 -30 -40 -44	dBm

3.4. Receiver

VBAT=3V

Table 5. Rx Characteristics

Characteristics	Test Conditions	Min	Typ	Max	Unit
Sensitivity, BER < 1000ppm	EU Band	—	-96	-93	dBm
Maximum input power	EU Band	—	—	15	dBm

4. Application Reference Schematic

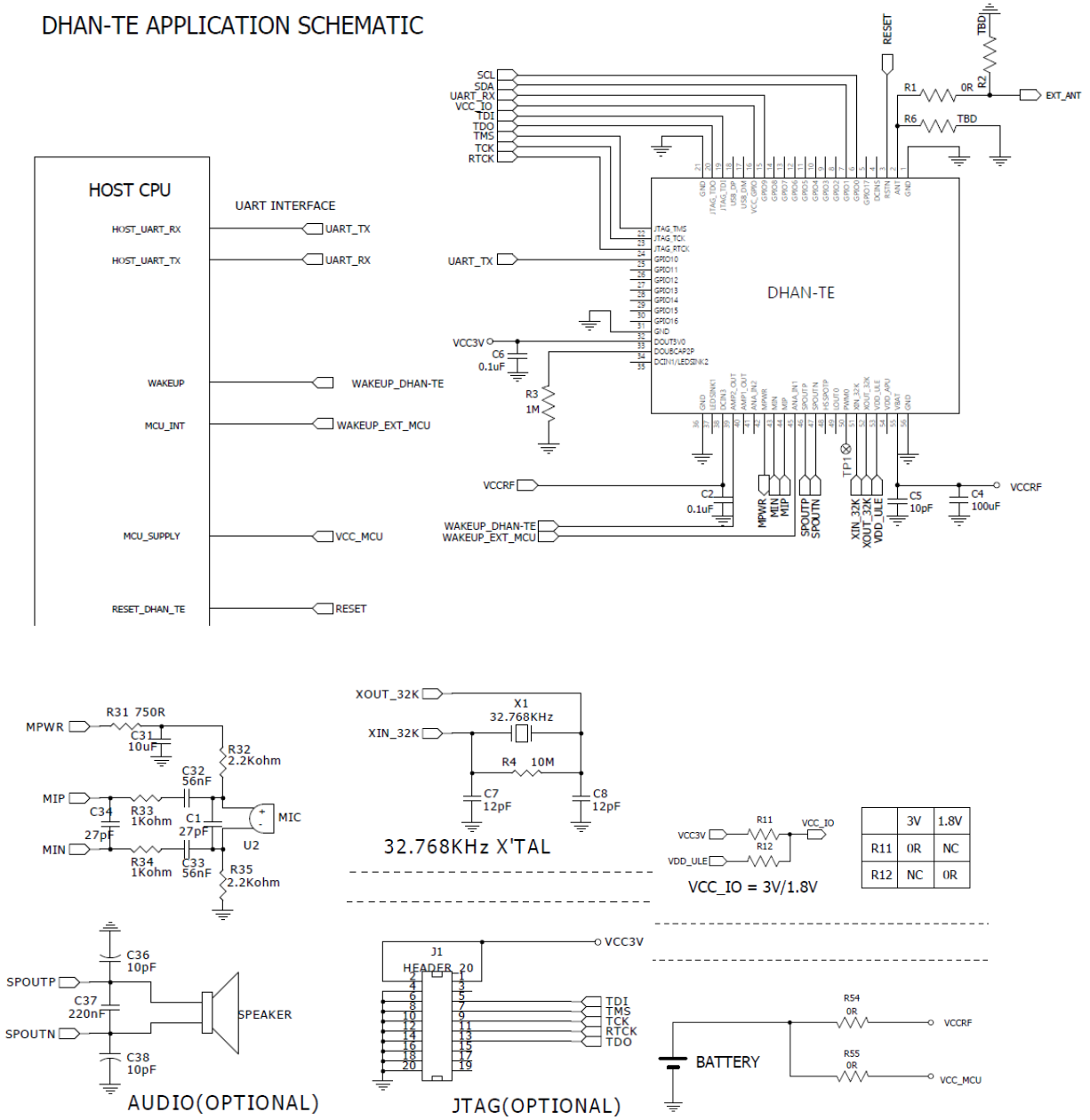

Figure 3. DHAN-TE Reference Schematic

5. Interfacing DHAN-TE with External MCU

5.1. RSTN Input

At power-up, the Application Host on the external MCU should hold pin 3 (RSTN Input) at logic Low until it is ready to establish communication (via UART) with the DHAN-TE. When ready, the Application Host should apply a rising edge (and leave at Logic High) and wait for the “Hello” indication from the DHAN-TE. If at some point later on the MCU cannot communicate with the DHAN-TE, it should apply a low going pulse of >100uS to reset the DHX101 on the DHAN-TE. Note that the RSTN pin is powered by the VBAT power domain. The minimum Logic High level is 0.6*VBAT.

5.2. UART, SPI Interfaces

Applications requiring a UART I/F and an SPI interface (for example, SmartVoice ULE applications), map the former to GPIOs 10 and 11 (Rx, Tx respectively) and the latter to GPIOs 6-9. Where only the UART I/F is required (as in the Reference Schematic provided in section 4), UART Rx is assigned to GPIO9 and Tx to GPIO10.

6. Application PCB Design Recommendations

It is recommended that unused pads on the Application PCB not be left as isolated islands of copper but rather be anchored via inner layers of the PCB. It is also recommended that GND vias be applied liberally in the vicinity of GND pins 1, 21, 36 and 56.

The following layout recommendations for embedding the DHAN-TE on the Application board:

- Implement a solid ground under the DHAN-TE module.
- Do not route signal traces under the module. Use the bottom layer for signal routing.

7. Assembly Information

7.1. Mechanical Drawing

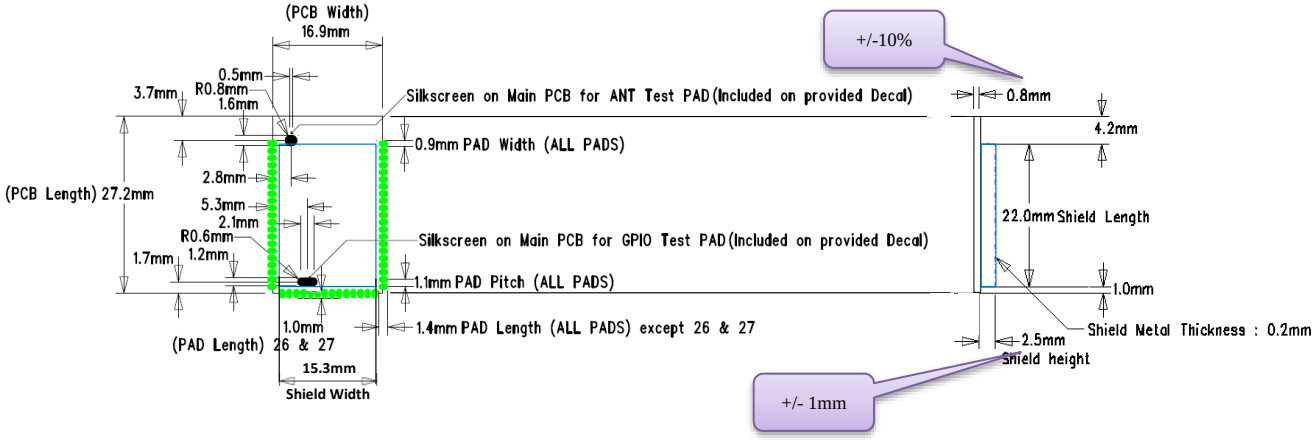

Figure 4. DHAN-TE mechanical drawing

7.2. PCB Footprint Detail

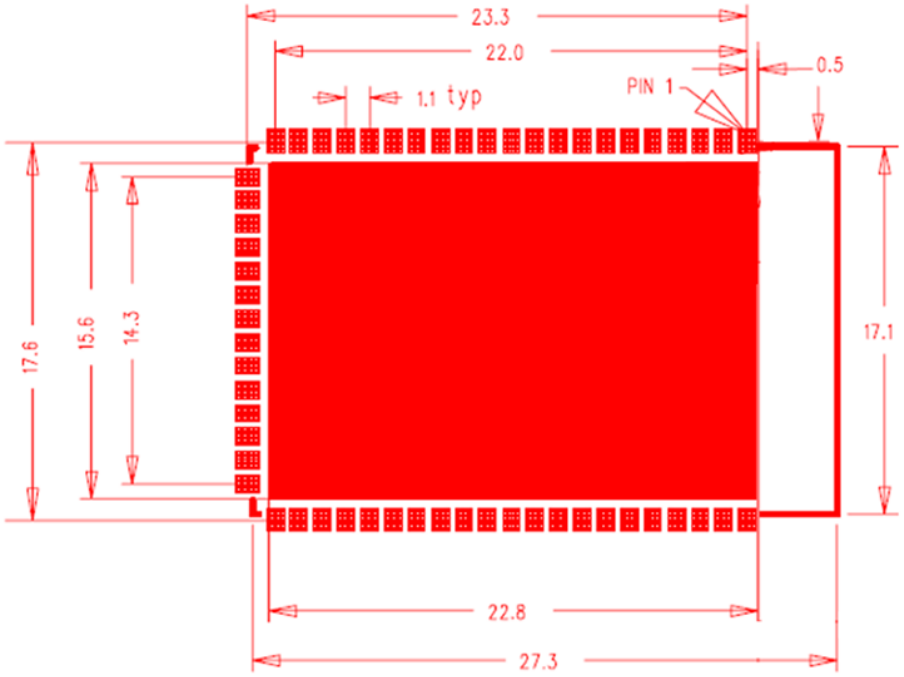

Figure 5. DHAN-TE PCB footprint

7.3. Pick & Place, Reflow

The DHAN-TE module uses a flat shield cover to facilitate a fully automatic assembly process. For backing and reflow recommendations, use MSL 3 in the JEDEC/IPC standard J-STD-20b. The temperature classification (TC) for the module is 245° C.

8. Supplementary Information

8.1. Labeling

Figure 6 shows the labeling details. The label is attached to the module shield.

1) Year
2) Week
3) 6-digit serial #
4) HW version
5) SW version

Figure 6. DHAN-TE Module Labeling Details

8.2. Handling Guidance

This module includes highly sensitive electronic circuity. Handling without proper ESD protection may damage the module permanently.

8.3. IPEI and EMC

Each DHAN-TE nodule is shipped to the customer with a unique IPEI, which serves as its DECT identity.

DHAN-TE will ship with an “EMC” of 0xFEB. This is the DSP Group “generic” EMC. The EMC setting identifies a Device as belonging to a specific group of ULE Devices/Hubs that utilize some proprietary signaling.

In either case, the customer is free to re-program these parameters.

8.4. Ordering Information

Part number: DHX101MDMDFED0AMI

9. Pre-Synaptics Revision History

Revision	Date	Description
1.0	August 4, 2021	Baseline release.
1.1	March 2, 2022	Ordering Info updated.

10. Revision History

Last Modified	Revision	Description
August 24, 2022	1	Preliminary rebrand as Synaptics.
September 24, 2022	A	Initial release to production; no change to content.

Copyright

Trademarks

Notice

Contact Us

Visit our website at www.synaptics.com to locate the Synaptics office nearest you.